In the Claims:

The claims are as follows:

1. (Previously Presented) An integrated circuit comprising:

a set of bitlines;

a set of data lines;

a coupling circuit that directly connects each respective data line to a first respective bitline or to a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline; and

a circuit that maintains said first respective bitline at a desired potential after said data line is coupled to said second bitline.

2. (Original) The integrated circuit of claim 1, wherein a number of said bitlines in said set of bitlines exceeds a number of data lines in said set of data lines.

3. (Previously Presented) The integrated circuit of claim 2, wherein each said data line is connected to only one of said bitlines and each said data line is connected to a different bitline.

4. (Original) The integrated circuit of claim 1, wherein said first respective bitline maintained at said desired potential is a failed bitline.

5. (Original) The integrated circuit of claim 1, wherein said desired potential is ground.

6. (Original) The integrated circuit of claim 1, wherein said data lines transfer data in parallel to said bitlines and said bitlines are coupled in parallel to one or more memory cells.

7. (Original) The integrated circuit of claim 1, wherein all said data lines in said set of data lines are arranged in a serial order and further including:

means for coupling each data line, after said data that has been coupled to said second respective bitline, to corresponding respective second bitlines.

8. (Original) The integrated circuit of claim 1, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines.

9. (Previously Presented) A method of replacing, in an integrated circuit having a multiplicity of data lines and a multiplicity of bitlines, a first bitline with a second bitline comprising:

providing a set of said multiplicity of said bitlines;

providing a set of said multiplicity of said data lines;

connecting each respective data line to a first respective bitline or to a second respective bitline through a switch and based on a steering signal supplied to said switch, said second respective bitline being adjacent to said first respective bitline; and

maintaining said first respective bitline at a desired potential after said data line is coupled to said second bitline.

10. (Original) The method of claim 9, wherein a number of said bitlines in said set of bitlines exceeds a number of data lines in said set of data lines.

11. (Previously Presented) The method of claim 10, wherein each said data line is connected to only one said bitlines and each said data line is connected to a different bitline.

12. (Original) The method of claim 9, wherein said first respective bitline maintained at said desired potential is a failed bitline.

13. (Original) The method of claim 9, wherein said desired potential is ground.

14. (Original) The method of claim 9, wherein said data lines transfer data in parallel to said bitlines and said bitlines are coupled in parallel to one or more memory cells.

15. (Previously Presented) The method of 9 wherein all said data lines in said set of data lines are arranged in a serial order and further including:

connecting each data line, after said data that has been connected to said second respective bitline, to corresponding respective second bitlines.

16. (Original) The method of claim 9, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines.

17. (Previously Presented) A content addressable memory comprising:

a set of bitlines;

a set of data lines, a number of said data lines less than a number of said bitlines;

a set of read lines, a number of said read lines equal to said number of said data lines, each said read line coupled to one corresponding bitline of said set of bitlines;

means for directly connecting each respective data line to a first-respective bitline or to a second respective bitline based on a steering signal, said second respective bitline being adjacent to said first respective bitline;

means for coupling each respective read line to a first respective read line or to a second respective read line based on said steering signal, said second respective read line being adjacent to said first respective read line; and

means for maintaining said first respective bitline at a known fixed state after said data line is connected to said second respective bitline.

18. (Previously Presented) The content addressable memory of claim 17, wherein all said data lines in said set of data lines are arranged in a serial order and all said read lines in said set of read lines are arranged in a serial order and further including:

means for directly connecting each respective data line, after said respective data line has been connected to said second respective bitline, to a corresponding third respective bitline, said third respective bitline immediately adjacent to said second respective bitline; and

means for directly connecting each respective read line, after said respective read line has been connected to said second respective read line, to a third respective read line, said third respective read line immediately adjacent to said second respective read line.

19. (Original) The content addressable memory of claim 17, further including:

one or none bitlines between said first respective bitline and said second respective bitline; and

one or none read lines between said first respective read line and said second respective read line.

20. (Previously Presented) The content addressable memory of claim 17, wherein said steering signal indicates which bitlines of said set of bitlines are failed bitlines and is derived from fuse latches.

21. (Previously Presented) The integrated circuit of claim 1, wherein said coupling circuit includes a latch stage connected to a switch stage.

22. (Previously Presented) The integrated circuit of claim 1, further including an additional coupling circuit that disconnects each respective data line connected to a second respective bitline by said coupling circuit from said second respective bitline and directly connects each respective data line to a third respective bitline based on said steering signal, said third respective bitline adjacent to said second respective bitline, said additional coupling circuit connected between said coupling circuit and said set of bitlines.

23. (Previously Presented) The integrated circuit of claim 22, wherein said coupling circuit includes a first latch stage connected to a first switch stage and said additional coupling circuit includes a second latch stage connected to a second switch stage.

24. (Previously Presented) The method circuit of claim 9, wherein said coupling circuit includes a latch stage connected to a switch stage.

25. (Previously Presented) The method of claim 9, further including providing an additional coupling, said additional coupling circuit disconnecting each respective data line connected to a second respective bitline by said coupling circuit from said second respective bitline and directly connecting each respective data line to a third respective bitline based on said steering signal, said third respective bitline adjacent to said second respective bitline, said additional coupling circuit connected between said coupling circuit and said set of bitlines.

26. (Previously Presented) The method of claim 25, wherein said coupling circuit includes a first latch stage connected to a first switch stage and said additional coupling circuit includes a second latch stage connected to a second switch stage

REMARKS

The Examiner has allowed claims 17-20. The Examiner has objected to claims 5, 13, 23 and 26 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim any intervening claims. Applicants gratefully acknowledge the Examiner's indication of allowable subject matter.

The Examiner rejected claims 1-4, 6-12, 14-16, 21, 22, 24 and 25 under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. (US 5,796,662) in view of Sauer (US 4,649,898).

The Examiner rejected claims 1-4, 6-12, 14-16, 21, 22, 24 and 25 under 35 U.S.C. 103(a) as being unpatentable over Kalter et al. (US 5,796,662) in view of Kirihata et al. (US 5,499,211). Applicants note, that there are no reasons for rejections of claims 2, 3, 6-12, 14-16, 21, 22, 24 and 25 given. Only claims 1, 4 and 9 appear to have been rejected based on Kalter et al. in view of Kirihata et al.

Applicants respectfully traverse the §103(a) rejections with the following arguments.

35 USC § 103 Rejections

The Examiner did not specifically mention claims 1 and 9 in his rejection but Applicants assume that the following rejections were meant to apply to claims 1 and 9.

As to Kalter in reference to claims 1 and 9, for both 35 USC §103(a) rejections the Examiner states that "Kalter discloses a wide-I/O DRAM chip with spare bitlines and a 'coupling circuit' that 'directly connects' adjacent first or second bitlines to a 'data line' based on a 'steering signal.' In one embodiment (not shown), the first and second bitlines are adjacent bitlines (col. 9, lines 19-24), although Kalter indicates that such an embodiment is not the most efficient. The first bitline may be still used as a replacement for the adjacent bitline on the side opposite the second bitline. The potential of the first bitline is presumably maintained at a desired potential, although means for maintaining bitline potential is apparently outside the scope of Kalter's description of bitline sparing logic."

First, Kalter does not teach or suggest "maintaining the first-bitline at a desired potential after the said data line is coupled to said second bitline" as Applicants claims 1 and 9 require The Examiner has stated that "presumably the first bitline is maintained at a desired potential" but there is no teaching in Kalter to do so. In fact Kalter teaches in col. 9, line 17 that defective lines are ignored.

Second, Kalter only indicates that with the "proper design adjustments" (see Kalter col. 9, line 16) his invention may be applied to bit-line redundancy. Applicants, maintain that this is a most ambiguous statement. Is Kalter talking about the memory design or his switching design? Further, there is no indication of what "proper design adjustments" actually comprise so this embodiment of Kalter is not enabled and cannot constitute prior art under 35 USC 102 (b).

As to Sauer in reference to claims 1 and 9 for the first 35 USC §103(a) rejection the Examiner further stated: "Sauer discloses maintaining bitlines at a desired potential to improve the operation of a memory array. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate Sauer's bitline potential maintaining means into Kalter's DRAM. Such incorporation would have been obvious because Sauer teaches that maintaining bitlines at desired potential improves the operation of a memory array."

First, the Examiner has acknowledged that Kalter does not teach or suggest any means for maintaining a disconnected bitline at a desired potential. Applicants point out that Sauer also does not teach or suggest maintaining a disconnected bitline at a desired potential. (1) the Sauer network would be disconnected from the bitline when the bitline was "switched out" by Kalter. (2) Sauer teaches a static-pull-up network connected to the bit lines which tends to maintain the bitlines at a given level during standby and a pull-up circuit, also connected to the bit lines, which is momentarily pulsed to precharge the bitlines to a desired level at the onset of each read cycle. (see Sauer col. 2 lines 5-8.) (2) The circuits of Sauer only hold the bitline to a desired potential (V_{DD}-V_{TN}) during standby or precharge to a desired level just before a read cycle. At other times the potential is allowed to decay. For example, col. 3 lines 58-59 of Sauer state "during an active cycle, pull the discharge bit lines towards (V_{DD}-V_{TN}) volts, albeit very slowly." Thus Sauer is not teaching "maintaining said first respective bit at a desired potential after said data line is coupled to said second bitline" as Applicants claims 1 and 9 require.

Second, Applicants can not find "improves the operation of a memory array" in Sauer and respectfully request the Examiner point out where Sauer teaches maintaining failed bitlines at a desired potential improves the operation of a memory array.

As to Kirihata in reference to claims 1 and 9 for the second 35 USC §103(a) rejection the Examiner further stated: "Kirihata discloses maintaining bitlines at a desired potential to improve the operation of a memory array. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate Kirihata's bitline potential maintaining means into Kalter's DRAM. Such incorporation would have been obvious because Kirihata teaches that maintaining bitlines at desired potential improves the operation of a memory array."

First, Kirihata actually teaches "a self current-limiting for a cross-fail between a bitline and a wordline" (see Kirihata abstract). (1) Kirihata's "bitline potential maintaining means" does not maintain potential at a desired level, but maintains current a desired level. The potential will vary depending upon the resistance of the short which is indeterminate before the short occurs. (2) Applicants point out that Kirihata's "bitline potential maintaining means" requires a short between the first bitline and a wordline to function. (3) Kalter is silent as to wordlines so it impossible to know if wordline to bitline shorts are possible in Kalter. Without knowing anything about wordlines in Kalter it is not proper to assume that Kirihata can be combined with Kalter.

Second, Applicants can not find "improves the operation of a memory array" in Sauer and respectfully request the Examiner point out where Sauer teaches maintaining failed bitlines at a desired potential improves the operation of a memory array.

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 9 are not unpatentable over either Kalter in view of Sauer or Kalter in view of Kirihata and are in condition for allowance. Since claims 2-8 and 21-23 depend from claim 1, and claims 10-16 and

24-26 depend from claim 9 Applicants respectfully maintain that claims 2-8, 10-16 and 21-26 are likewise in condition for allowance.

As to claims 2 and 10, Kalter is not showing more bitlines per column than the number of data lines. Only FIGs 2 and 3A of Kalter show arrays (FIG. 1 is prior art). Kalter in FIG. 2 is showing one more data line than there are bitline inputs or bit line outputs. Kalter FIG. 3A shows no data lines.

As to claims 4 and 12, Applicants point out that Kalter, as described *supra*, teaches ignoring failed bitlines.

As to claims 21 and 24, Applicants cannot see how a sense amplifier has any latch function at all. Any input present to a sense amplifier generates an immediate output and the input is not latched (there is no internal node latching the input value).

As to claims 22 and 25, Applicants point out that the switches of Kalter can only connect either a first or a second bitline and cannot connect the either the first or the second bitline to a third bitline. (see Kalter FIG. 2).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

Respectfully submitted,
FOR: Batson et al.

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